WHAT IS CLAIMED IS:

1. A communications interface apparatus, comprising:

a register circuit storing data to be transferred to a host computer;

a first memory storing first information indicating a specific address of the register circuit and representing an access to the communications interface apparatus executed by the host computer for a data transfer;

a second memory storing second information, sent from the host computer in association with the first information stored in the first memory, to be written into the register circuit at the specific address indicated by the first information stored in the first memory; and

a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed.

2. A communications interface apparatus according to Claim 1, wherein the control circuit performs the information writing operation to write the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface

apparatus is changed from a low power consumption mode to a regular operation mode.

3. A communications interface apparatus according to Claim 2, wherein the control circuit performs an information reading operation for reading the first and second information written in the first and second memories, respectively, in chronological order of the accesses executed and an information transfer operation to transfer the first and second information read from the first and second memories, respectively, to the register circuit in chronological order of the accesses executed, when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode.

4. A communications interface apparatus according to Claim 3, wherein each of the first and second memories comprises a first-in and first-out memory including a specific number of buffer areas into which data from the host computer is written, and the control circuit conducts the information writing operations with respect to the first and second memories in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each

other.

5. A communications interface apparatus according to Claim 4, wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation, and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal.

6. A communications interface apparatus according to Claim 5, wherein the control circuit transfers the first and second information directly to the register circuit, without buffering the first and second information in the first-in and first-out memories of the first and second memories, in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode.

7. A communications interface apparatus according

to Claim 6, wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths.

8. A communications interface apparatus according to Claim 7, wherein the control circuit comprises:

a data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer;

a data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the write control circuit block starts writing the first and second information into the first and second memories, respectively;

a status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to

output a status signal representing the memory statuses detected; and

a selection control circuit block configured to control the selection circuits included in the respective first and second memories in accordance with a status as to whether the operation mode of the communications interface apparatus is the low power consumption mode and the status signal output from the status detecting circuit block.

9. A communications interface apparatus according to Claim 1, wherein the register circuit, the first and second memories, and the control circuit are integrated into a single integrated chip.

10. A communications interfacing method comprising the steps of:

storing in a register circuit data to be transferred to a host computer;

storing in a first memory first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer, and storing in a second memory second information, sent from the host computer in association with the first information stored in the first memory, to be written into the register circuit at

the specific address indicated by the first information stored in the first memory; and

performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed.

11. A communications interfacing method according to Claim 10, wherein the performing step performs the information writing operation to write the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

12. A communications interfacing method according to Claim 11, further comprising the steps of:

executing an information reading operation with the control circuit for reading the first and second information written in the first and second memories, respectively, in chronological order of the accesses executed by the performing step; and

conducting an information transfer operation with the control circuit for transferring the first and second

information read from the first and second memories, respectively, performed by the executing step to the register circuit in chronological order of the accesses executed, when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode.

13. A communications interfacing method according to Claim 12, wherein each of the first and second memories includes a first-in and first-out memory including a specific number of buffer areas into which data from the host computer is written by the performing step, and

wherein the performing step performs the information writing operations with respect to the first and second memories in synchronism with each other and the executing step executes the information reading operations with respect to the first and second memories in synchronism with each other.

14. A communications interfacing method according to Claim 13, wherein the performing step uses a first clock signal for synchronizing the information writing operation and the executing step uses a second clock signal for synchronizing the information reading operation, and

wherein a first frequency of the first clock signal is

greater than a second frequency of the second clock signal.

15. A communications interfacing method according to Claim 14, wherein the data writing operation performed by the performing step transfers the first and second information directly to the register circuit without buffering the first and second information into the first-in and first-out memories of the first and second memories, in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information written in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode.

16. A communications interfacing method according to Claim 15, further comprising the steps of:

generating a selection control signal using the control circuit;

selecting one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on

an exclusive basis according to the selection control signal; and

outputting corresponding data to the register circuit through one of the first and second data paths selected.

17. A communications interfacing method according to Claim 16, wherein the performing step instructs the information writing operation to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer,

wherein the executing step instructs the information reading operation to start reading the first and second information from the first and second memories, respectively, upon a time the information writing operation starts writing the first and second information into the first and second memories, respectively, and

wherein the method further comprises the steps of:

detecting memory statuses of the first-in and first-out memories included in the respective first and second memories, using the control circuit;

outputting a status signal representing the memory statuses detected; and

controlling the selecting step by the control circuit in accordance with a status as to whether the operation mode

of the apparatus is the low power consumption mode and the status signal output from the status detecting circuit block.

18. A communications interfacing method according to Claim 10, wherein the register, the first and second memories, and the control circuit are integrated into a single integrated chip.

19. An optical disk drive apparatus, comprising:

an optical disk drive mechanism; and

an interface circuit for interfacing communications between the optical disk drive mechanism and a host computer, the interfacing circuit comprising:

an input terminal for receiving data sent from the host computer;

a data processor configured to perform a predetermined data processing operation to the data received through the input terminal;

a clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation;

an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to

change an operation mode from a regular operation mode to a low power consumption mode;

a buffering circuit block configured to buffer the data received through the input terminal, the buffering circuit block including:

a first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory, and

a second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory; and

a path selection controller configured to control the buffering circuit clock to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode.